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Title of Invention:	METHOD AND APPARATUS FOR ACCELERATING THE VERIFICATION OF APPLICATION SPECIFIC INTEGRATED CIRCUIT DESIGNS
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/Message Digest	Multi Part/.zip	Pages (if appl.)
1	Petition automatically granted by EFS	Hyduke_4507P3174_Pett.pdf	842026 3800e9115173015d88d0fa263ab02df925b6 9995	no	3
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	32178 23c258dc0b74998f288003e8fb10372a5e35 3431	no	2
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